[CLAIMS]

What is claimed is:

1. A semiconductor memory device operable in synchronization with an external clock signal comprising:

a data transfer circuit, having a first transfer mode and a second transfer mode, for transferring data in synchronization with rising and falling edges of an external clock signal in the first transfer mode, and for transferring data in synchronization with only one of the rising and falling edges in the second transfer mode.

2. A semiconductor memory device as set forth in claim 1, wherein the data transfer circuit switches the first and second transfer modes in response to a mode switch signal.

3. A semiconductor memory device as set forth in claim 2, wherein the mode switch signal is generated on the basis of a setting signal input from outside of the device.

4. A semiconductor memory device as set forth in claim 3, further comprising a register to latch the setting signal.

5. A semiconductor memory device as set forth in claim 4, wherein the register is arranged in a mode register.

6. A semiconductor memory device as set forth in claim 2, wherein the mode switch signal is input to a switch signal input terminal.

7. A semiconductor memory device as set forth in claim 1,

wherein the second transfer mode transfers the data in synchronization with the rising edge of the external clock signal.

8. A semiconductor memory device as set forth in claim 2, wherein the data transfer circuit has a data input converter, for simultaneously transferring parallel data converted from serial data which are input serially in the first transfer mode, and for sequentially transferring the serial data in the second transfer mode.

9. A semiconductor memory device as set forth in claim 8, wherein the data transfer circuit has a data input clock generating circuit, for generating a first clock signal in the first transfer mode or a second clock signal in the second transfer mode in response to the mode switch signal, and for transmitting the first clock signal or the second clock signal to the data input converter.

10. A semiconductor memory device as set forth in claim 8, wherein the data transfer circuit has a write control circuit, for generating a first write enable signal to simultaneously transfer the parallel data to a memory cell array in the first transfer mode, and for generating a second write enable signal to sequentially transfer the serial data to the memory cell array in the second transfer mode.

11. A semiconductor memory device as set forth in claim 8, further comprising a column address counter which can change a timing to count up a column address in response to the mode switch signal.

12. A semiconductor memory device as set forth in claim 11,

wherein the column address counter comprises:

a clock generating circuit supply a first internal address generating clock and a second internal address generating clock;

a first address generating section generation a first internal address in synchronization with the first internal address generating clock; and

a second address generating section generating a second internal address in synchronization with the second internal address generating clock.

13. A semiconductor memory device as set forth in claim 12, wherein the clock generating circuit comprises a clock generator and a frequency divider, the clock generator generating an internal clock in response to the external clock, the frequency divider receiving the internal clock and generating a divided clock, and wherein the clock generating circuit outputs the internal clock as the first internal address generating clock in the first transfer mode, and outputs the divided clock as the first internal address generating clock and the internal clock as the second internal address generating clock in the second transfer mode.

14. A semiconductor memory device as set forth in claim 13, further comprising a burst counter which starts counting the internal clock according to a write or read command, and deactivates the clock generator when the predetermined number of the internal clocks is counted.

15. A semiconductor memory device as set forth in claim 14, wherein the burst counter comprises a burst length conversion circuit for converting the predetermined number of the internal

clocks in response to the mode switch signal.

16. A semiconductor memory device as set forth in claim 1, wherein the data transfer circuit transfers data to a memory cell array when the data is the write data.

17. A method of controlling a semiconductor memory device operable in synchronization with an external clock signal comprising:

transferring data in synchronization with both of rising and falling edges of the external clock signal in a first transfer mode; and

transferring the data in synchronization with one of the rising and falling edges in a second transfer mode.

18. A method as set forth in claim 17, wherein the first and second transfer modes are switched in response to a switch signal which is generated on the basis of a setting signal input from outside of the device or directly input from the outside.

19. A method as set forth in claim 17, wherein the data is transferred in synchronization with the rising edge of the external clock signal in the second transfer mode.

20. A method as set forth in claim 17, wherein the step of transferring includes executing a serial to parallel conversion of a plurality of data serially input and simultaneously transferring converted parallel data in the first transfer mode, and sequentially transferring a plurality of data in the second transfer mode.

21. A method as set forth in claim 20, wherein the step of

transferring includes switching, in response to a switch signal, whether a plurality of data are simultaneously transferred after the serial to parallel conversion or are sequentially transferred.

22. A method as set forth in claim 20, wherein the step of transferring includes outputting a first write enable signal to a write amplifier in the first transfer mode and outputting a second write enable signal in the second transfer mode in response to a switch signal when the data is transferred to a memory cell array.

23. A method as set forth in claim 20, wherein the step of transferring includes changing a timing to count up a column address in response to a switch signal.

24. A method as set forth in claim 17, wherein the second transfer mode is selected when the data is written in a test mode.

25. A column address counter for counting up a column address comprising:

a timing change circuit to switch a timing for counting up the column address in response to a mode switch signal which indicates a first transfer mode or a second transfer mode, wherein data is transferred in synchronization with both of rising and falling edges of a clock signal in the first transfer mode, and the data is transferred in synchronization with only one of the rising and falling edges in the second transfer mode.

26. A column address counter as set forth in claim 25, further comprising:

a clock generating circuit supplying a first and second internal address generating clocks;

a first address generating section generating a first internal address in synchronization with the first internal address generating clock; and

a second address generating section generating a second internal address in synchronization with the second address generating clock.

27. A column address counter as set forth in claim 26, wherein the clock generating circuit comprises a clock generator and a frequency divider, the clock generator generating an internal clock in response to an external clock, the frequency divider receiving the internal clock and generating a divided clock, and wherein the clock generating circuit outputs the internal clock as the first internal address generating clock in the first transfer mode and outputs the divided clock as the first internal address generating clock and the internal clock as the second internal address generating clock in the second transfer mode.

28. A semiconductor memory device of a double data rate type for reading data in response to rising and falling edges of a clock having an operating mode to immediately read the data with a read command.

29. A semiconductor memory device as set forth in claim 28, wherein in the operating mode the data is outputted on an access time of a column address strobe signal.

30. A semiconductor memory device of a double data rate type for reading data in response to both of rising and falling edges of a clock having a single data rate mode for reading the data in response to one of the rising and the falling edges of the clock.

31. A semiconductor memory device as set forth in claim 30, wherein in the single data rate mode the data is outputted on an access time of a column address strobe signal.

32. A semiconductor memory device as set forth in claim 30, wherein in the single data rate mode the data is outputted between a rise timing of the clock to the access time of the column address strobe signal.

33. A semiconductor memory device as set forth in claim 30, the single data rate mode is used in a test in a wafer state of the semiconductor memory device.

34. A semiconductor memory device of a double data rate type for writing data in response to both of rising and falling edges of a clock having an operating mode for immediately writing the data after a write command is received.

35. A semiconductor memory device as set forth in claim 34, wherein in the operating mode only the data which is received at substantially the same time the write command is input, is written.

36. A semiconductor memory device of a double data rate type for writing data in response to both of rising and falling edges of a clock having a single data rate mode to write data in response to one of the rising and falling edges of the clock.

37. A semiconductor memory device as set forth in claim 36, wherein in the single data rate mode only the data which is input Almost simultaneously with the write command, is written.

38. A semiconductor memory device as set forth in claim 36, wherein in the single data rate mode the write data is inputted in response to a data strobe signal.

39. A semiconductor memory device as set forth in claim 36, wherein the single data rate mode is used in a test in a wafer state of the semiconductor memory device.

40. A semiconductor memory device as set forth in claim 1, wherein the semiconductor memory device is a synchronous dynamic random access memory.